

IN THE CLAIMS:

Please amend claims 5 and 6 as follows:

5. (Currently Amended) An electronic phase-locked loop for the jitter-attenuated generation of an ~~high-frequency~~ output clock signal which is phase-synchronous with respect to a reference clock signal, ~~having comprising a circuit having:~~

a digitally controllable oscillator ~~with,~~

a drive circuit; ~~for~~

~~which digitally sets~~ setting the output clock signal of the digitally controllable oscillator ~~until so that~~ a phase error between the output clock signal and a reference clock signal, ~~which is specified discreetly by a counter reading of a counter,~~ is zero,

a digital phase detector; ~~for~~

~~which compares~~ the output clock signal of the oscillator with the reference clock signal ~~via a PI filter and the drive circuit,~~

an analog phase detector ~~in parallel with said digital phase detector,~~

a lock detection circuit for avoiding a phase quantization error, and

~~said circuit activating the analog phase detector to run simultaneously with said digital phase detector if the phase error specified by the counter reading is zero,~~

the activated analog phase detector regulating the output clock signal of the digitally controllable oscillator in a continuously variable manner until the respective clock signal edges of the output clock signal and of the reference clock signal are fully synchronous,

the ~~lock~~ lock detection circuit deactivating the analog phase detector and continuously checking and activating the digital phase detector if until the phase error between the output clock signal and the reference clock signal ~~does not exceeds~~ a specific phase error.

6. (Currently Amended) The electronic phase-locked loop as claimed in claim 5, ~~wherein the further including a PI filter has~~ with an integral regulation, a linear regulation and an addition and amplifier stage, which is driven by the analog phase detector ~~via a line.~~